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WAVELET PACKET TRANSFORM BASED ECG SIGNAL FILTERING IMPLEMENTED IN RECONFIGURABLE HARDWARE STRUCTURE

Zoltán GERMÁN-SALLÓ[1], Cristina LUTEAN[2],

[1,2] *"Petru Maior" University of Tîrgu Mureş*
Nicolae Iorga Street, no.1, 540088, Tîrgu Mureş, Romania
[1]zoltan.german-sallo@ing.upm.ro@
[2]cristinalutean@yahoo.com

Abstract

This work describes an implementation of a digital signal processing module for filtering ECG signals in a reconfigurable hardware structure (FPGA). The filtering structure, a Wavelet Packet decomposition based decomposition is implemented in Simulink with Xilinx blocksets. The used structure is a Diligent's Xilinx University Program Virtex-II Pro Development System. The integrated Xilinx ISE software provides automatic generation of HDL code directly from the System Generator blocks that is then mapped to the Xilinx FPGA. This code is synthesized and implemented in a Xilinx FPGA in order to perform a hardware co-simulation. In order to evaluate the filtering procedure signal to noise ratio and root mean squared error are measured.

Key words: Wavelet Packet Transform, thresholding, FPGA, Simulink, System Generator

1. Introduction

The extraction of parameters from a noisy electrocardiogram (ECG) remains an important task for the biomedical engineering community. The ECG is the representation of the potential difference between different points on a body surface that originate from the electrical activity of human heart and it's considered as a nonstationary signal. Time-frequency transforms as Discrete Wavelet Transform (DWT) and Wavelet Packet Transform (WPT) are usually known as very useful in non-stationary signal's analysis due to their multiresolution capabilities. Wavelet Transform (WT) based filtering is now a common practice for denoising of signals having multiresolution characteristics such as the ECG signal [8], [2], [3].

MATLAB is a very useful tool for algorithm development, data analysis, a large number of the algorithms used today in digital signal processing originates as MATLAB models. Simulink is a graphical tool, which lets the user to design the architecture and simulate the timing and behaviour of the whole system in an interactive way. Xilinx System Generator is a MATLAB/Simulink-based design tool for Xilinx's line of FPGAs which offers block libraries that plugs into Simulink tool (containing bit-true and cycle-accurate models of their FPGAs particular mathematic, logic, and digital signal processing functions) [4], [5].

2. The Discrete Wavelet Packet Transform

The wavelet transform is a decomposition of the signal as a combination of a set of basis functions, obtained by means of dilation a and translation b of a prototype wavelet $\psi(t)$. The wavelet transform (WT) of signal $x(t)$ is defined as [1]:

$$W_a x(b) = \frac{1}{\sqrt{|a|}} \int_{-\infty}^{+\infty} x(t) \cdot \psi\left(\frac{t-b}{a}\right) dt \qquad (1)$$

For discrete time-signals, is defined the Discrete Wavelet Transform (DWT) where the mother wavelet is discretized (that means discrete dilations and translations)in a following matter [6]:

$$\psi_{(s,l)}(x) = 2^{-\frac{s}{2}} \psi\left(2^{-s} x - l\right) \qquad (2)$$

The scale index *s* indicates the wavelet's width, and the location index *l* gives its position. Usually, the scales *s*, *l* are integer powers of two; in this case we deal with the dyadic wavelet transform which can be implemented with Mallat's algorithm in an octave filter bank [8].

The Discrete Wavelet Transform decomposition of the signal into different frequency bands [3] can be obtained by successive high-pass and low-pass

filtering (digital FIR filters structures) of the signal in time domain followed by downsamplig to eliminate the redundancy (to keep the number of coefficients correlated to the represented frequency band).

Wavelet packet analysis is a generalization of wavelet analysis providing a redundant decomposition procedure, using these basic equations:

$$\varphi(t) = \sqrt{2}\sum_{k=-\infty}^{+\infty} h_k \varphi(2t+k),$$

$$\psi(t) = \sqrt{2}\sum_{k=-\infty}^{+\infty} g_k \varphi(2t+k) \qquad (3)$$

The wavelet packet method is a generalization of wavelet decomposition that offers a richer range of possibilities for signal analysis. For *n* levels of decomposition the WPD produces *2n* different sets of coefficients (or nodes) as opposed to *(3n + 1)* sets for the DWT. In wavelet packet analysis, the details as well as the approximations can be split.

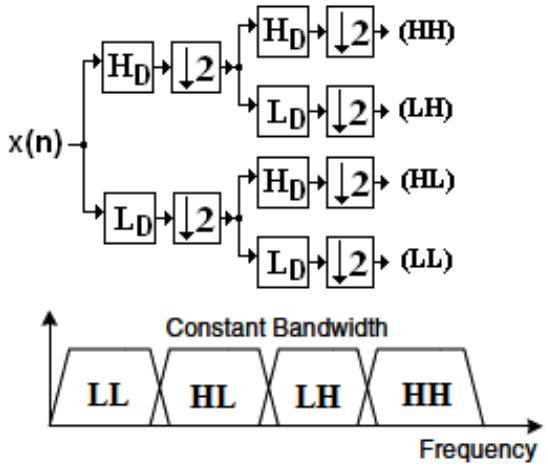

Fig. 1 WPT decomposition

Each component in this wavelet packet tree can be viewed as a filtered component with a bandwidth of a filter decreasing with increasing level of decomposition. At the top of the tree, the time resolution of the WP components is good but at the bottom the frequency resolution is increased. As a result, the wavelet packet analysis provides better control of frequency resolution for the decomposition of the signal [13]. After a WPT decomposition the signal is split in equally dimensioned frequency bands, called subbands and a large number of signal processing actions can be performed. Acting independently in these subbands, more accurate processing results can be obtained. This dyadic division of the bandwidth (splitting both approximation and detail components) could be the key of subband filtering techniques which allow independent processing in these subbands, tis could become a great advantage in certain domains.

3. Xilinx System Generator

Hardware description languages (HDLs) allow designers to specify the tasks at a higher level than logic gates when work with reconfigurable hardware structures as FPGAs. within the HDL environment the level of abstraction is very low, the difficulty increases as the design becomes more complex.

System Generator is a MATLAB/Simulink-based design tool for Xilinx's line of FPGAs and replaces the traditional Hardware Description Language (HDL) design, without requiring a detailed knowledge of this lower level, complex language. In addition, this graphical tool allows an abstraction of the design through the use of available System Generator blocks and subsystems. Because of the graphical nature of System Generator, the overall design is able to be viewed as a modular system with a high level of abstraction which does not require HDL code from the designer [9].

System Generator provides blocks for building the desired model, and HDL code generation for implementation. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. A lot of numbers (depending on the version) of digital signal processing building blocks are provided in the Xilinx DSP blockset for Simulink. System Generator provides many features such as System Resource Estimation to take full advantage of the FPGA resources, Hardware Co-Simulation and accelerated simulation through hardware in the loop co-simulation; which give many orders of simulation performance increase. the integration with Simulink, provides for the hardware design and verification to be performed from within the same environment as the mathematical system model, reducing both the required design time and hardware resources [11], [14], [15].

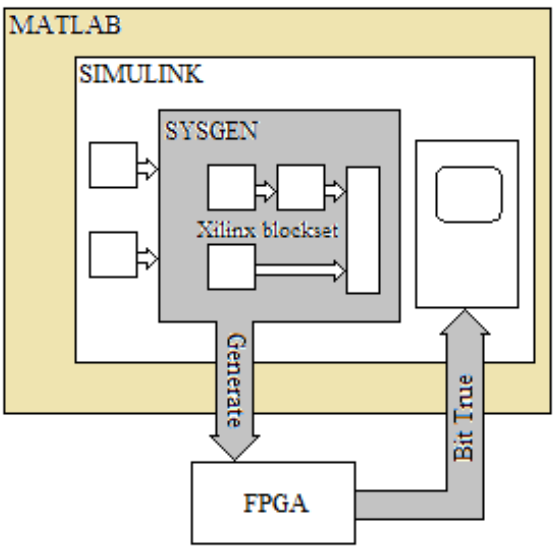

Fig. 2 The System Generator

4. The procedure

The proposed non-linear filtering procedure acts by thresholding the coefficients as we can see on figure 3. [6], [7]. The general de-noising procedure involves three steps, decomposition, thresholding detail coefficients and reconstruction of the signal. These steps are presented on figure 3.

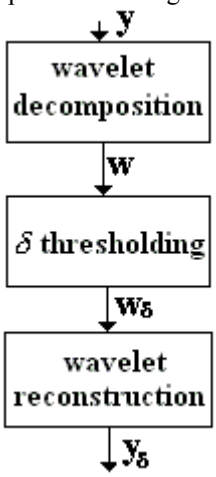

Fig 3 The nonlinear filtering procedure

The proposed model for a second level WPT decomposition based filtering is presented on figure 3. The model is carried out in Simulink environment, using the specific Xilinx blocks. The used input signal is from MIT-BIH database, mapped in a .mat file, representing ECG signal with normal sinus rhythm. In order to evaluate the filtering process, a known normally distributed noise is added. The used analyzing wavelet function was 'db4'and excepting the lower frequency component, all others were passed through a level-specific threshold. After that the signal was recomposed from the theresholded coefficients, obtaining the filtered signal. Working independently in subbands, different thresholds for different components can be applied in order to accomplish a very specific filtering task. Wavelet shrinkage is usually performed using one of two predominant thresholding versions [12], [9]. Applying the hard threshold coefficients below a threshold value, determined by the noise variance, are removed. The soft thresholding method shrinks the wavelet coefficients above and below the threshold reducing coefficients toward zero [3]. The process of denoising is necessarily lossy, the denoised signal is irreversibly different than the noisy signal. The blocks containing the thersholding values are also implemented in the Simulink model [10], [13]. The Xilinx Integrated Software Environment (ISE) is a powerful design environment that is working in the background when implementing System Generator blocks. The synthesis of these modules creates netlist files which serve as the input to the implementation module. After generating these files, the logic design is converted into a physical file that can be downloaded on the target device. The software also provides a simulation tool where the functionality, behaviour and timing can be verified for users that are familiar with the ISE software.

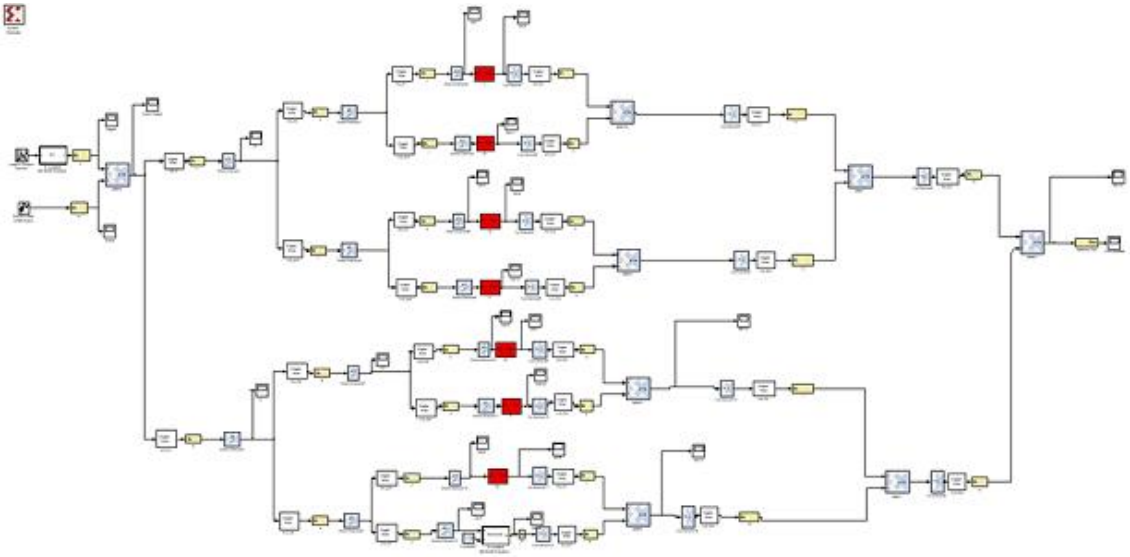

Fig. 4 The model of proposed procedure

5. Results

In the filtering process the soft thresholding method was applied, because usually gives better results. The proposed filtering procedure was realized in good conditions, the performances were measured through absolute filtering errors, the noisy and filtered signals obtained after hardware co-simulation can be viewed in figure 5.

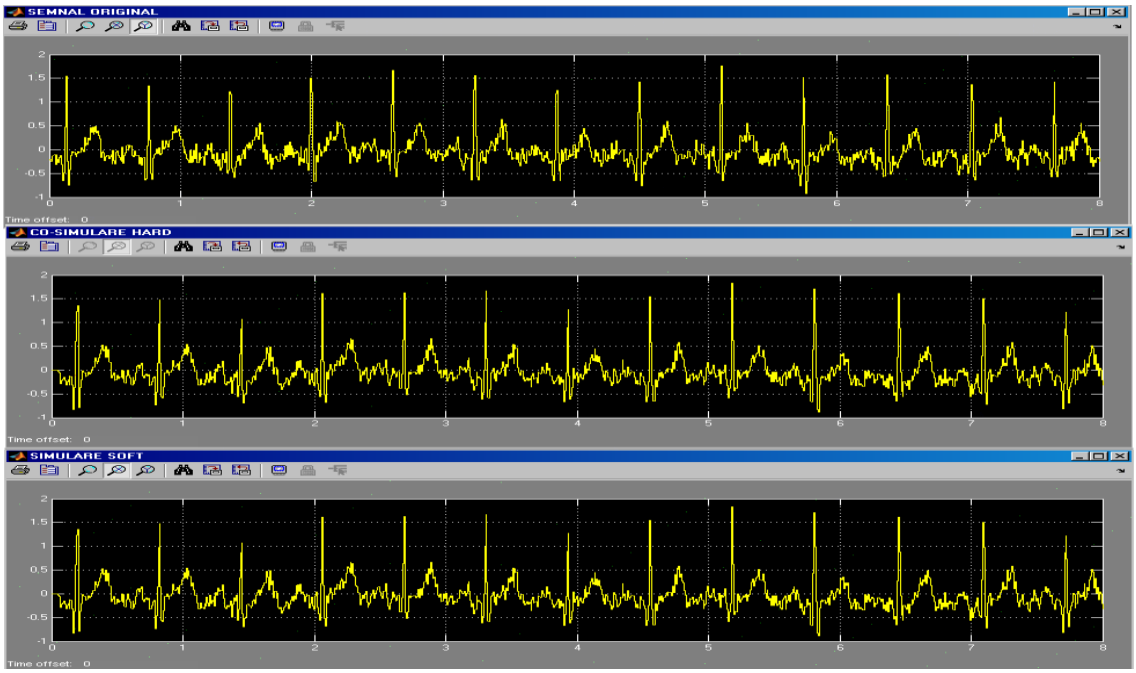

Fig. 5 Soft and hard thresholded based filtering results in hardware co-simulation

Conclusions

The System Generator Environment allows to explore the design options in terms of size and speed to fulfil the design constraints. This is due to the fact that System Generator allows the algorithms designed to be implemented from within the Simulink environment.

References

[1] Abramovich F., Bailey T. C., and Sapatinas T. (2000), Wavelet analysis and its statistical applications, *Journal of the Royal Statistical Society*, Series D , vol. 48, pp. 1–30.

[2] Barber S., Nason G. P., and Silverman B. W. (2002), Posterior probability intervals for wavelet thresholding, *Journal of the Royal Statisitcal Society*, Series B, vol. 64, pp. 189–205.

[3] Burrus C. S., Gopinath R. A. and Guo H. (1998), *Introduction to Wavelets and Wavelet Transforms*, Prentice Hall.

[4] Dick C, Krikorian Y.(1999) A System-Level Design Approach for FPGA-Based DSP Implementations", DSP World, Spring.

[5] Lamár K. and Morva G. (2013), Hardware and Software Functions of Standalone Field Data Acquisition Devices for the Low Voltage Power Distribution Grid, *Carpathian Journal of Electronic and Computer Engineering* , vol. 6/1, pp. 22-27.

[6] Lotri U., (2004), Wavelet based denoising integrated into multilayered perceptron, *Neurocomputing*, vol. 62, pp. 179–196.

[7] M. Weeks (2007), *Digital Signal Processing using Matlab and Wavelets*, Infinite Science Press LLC.

[8] Mallat S. (2001), *A Wavelet Tour of Signal Processing*, Academic Press.

[9] Manly B.F.G. (2005), *Multivariate Statistical Methods: A Primer*, Chapman & Hall/CRC, Boca Raton.

[10] Meyer-Baese U. (2007) *Digital Signal processing with Field Programmable Gate Arrays*. Springer Verlag Berlin.

[11] Ownby M, Mahmoud W.H. A Design Methodology for Implementing DSP with Xilin System Generator for Matlab. IEEE International Symposium on System Theory, 2003,pp. 404- 408

[12] Percival D. B. and Walden A. T. (2000), *Wavelet methods for time series analysis*, Cambridge University Press, Cambridge.

[13] Ranjan P.(2008) Implementation of FIR Filters on FPGA. Master Thesis, Department of Electronics and Communication Engineering, Thapar University, Punjab,India,

[14] Soltani S., Boichu D., Simard P., and Canu S. (2000), The long-term memory prediction by multiscale decomposition, *Signal Processing*, vol. 80, pp. 2195–2205.

[15] Wang YS.(2005) Implementation of digital filter by using FPGA," *Bachelor of Engineering*, Curtin University of Technology